REMARKS

I. Status of Claims

The Applicant has carefully considered the final Office Action dated December 24, 2008, and the references it cites. Currently, claims 1-10 are pending in this application. In the Office Action, the Examiner rejects:

- claims 1-3 and 6-8 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,639,915 to Tsztoo et al. (*Tsztoo*) in view of U.S. Patent No. 6,639,915 to Kuehnel et al. (*Keuhnel*); and
- claims 4-5 and 9-10 as being unpatentable over *Tsztoo* in view of *Kuehnel* and in further view of U.S. Patent No. 6,201,789 to Witkowski et al. (*Witkowski*).

In response, the Applicant submits the foregoing amendments and the following remarks.

II. Objections to the Specification

In the Office Action, the Examiner objected to the abstract because the content allegedly recites the claims. The Examiner notes that the content of the abstract ***should*** be such as to enable the reader thereof, regardless of his or her degree of familiarity with patent documents, to determine quickly from a cursory inspection of the nature and gist of the technical disclosure. In response, the Applicant notes the Examiner indicates that content of the abstract is ***permissive***. Accordingly, the Applicant kindly declines the opportunity to amend the abstract based on the Examiner's request.

III. Claim Rejections under 35 U.S.C. § 103(a)

Claim 1 recites a symbol buffer memory device comprising, *inter alia*, a buffer memory for storing the symbol data for the logical channel according to input sequences so that the symbol data of the logical channels are stored in a continuous arrangement and a start address table for storing address information according to the logical channels, each of the address information indicating a location of initial symbol data corresponding to each of the logical channels from among the symbol data stored in the buffer memory.

The Applicant respectfully submits that *Tsztoo* fails to describe a start address table as recited in claim 1. To reject claim 1, the Examiner contends the channel address memory related to FIG. 9 is analogous to the start address table as recited in claim 1. However, *Tsztoo*

merely describes that "CHANNEL # values generated by the CAM 920 are applied to a channel address memory 922." *See Tsztoo at 14:63-64.* Further, the "channel address memory includes storage locations corresponding to various CHANNEL# values." *See Tsztoo at 14:64-65.* That is, *Tsztoo* merely describes storage locations corresponding to various CHANNEL# values. By contrast, claim 1 recites a start address table for storing address information according to the logical channels, each of the address information indicating a location of initial symbol data corresponding to each of the logical channels.

The Applicant notes that *Tsztoo* also fails to describe a buffer memory for storing the symbol data for the logical channel according to input sequences so that the symbol data of the logical channels are stored in a continuous arrangement. The Examiner continues to allege that *Tsztoo* teaches a buffer memory. To support this proposition, the Examiner cites to FIG. 9 and the description related to CHANNEL_ADD. The Applicant notes that the description the Examiner relies upon is a description of a third embodiment that describes content addressable memory (CAM) that "generates a voice channel identification value (CHANNEL#) in response to address and data values receive [sic] from buses." *See Tsztoo at 14:23-25.* Further, "[t]he voice channel identification information is applied as a number of index fields to CAM 920 to generate a channel identification number (shown as CHANNEL#)." *See Tsztoo at 14:34-36.* The "CHANNEL# values generated by the CAM 920 are applied to a channel address memory 922" to generate a channel base address ($BASE_{13}$ ADD). *See Tsztoo at 14:63-15:5.* By adding the channel base address ($BASE_{13}$ ADD) to an offset value (OFFSET), *Tsztoo* generates the channel address ($CHAN_{13}$ ADD) with the channel address generator 924. *See Tsztoo at 15:11-16.*

Tsztoo further describes that additional functions require the "the CAM address system 910 to provide 'non-voice' data that is used to program the operation of the CAM 920." *See Tsztoo at 15:26-28.* In particular, *Tsztoo* describes masking schemes because the data in the VPBM is non-contiguous and the "the request arbiter 928 controls the address and data MUXes (930 and 932) according to received request values." *See Tsztoo at 15:44-47.* Based on the "applied request values, address values on the address bus will be applied to the a [sic] VPBM 934 and a data bus will be coupled to the VPBM 934." *See Tsztoo at 15:47-49.* Stated differently, it appears that *Tsztoo* describes non-voice data not related to a logical channel and voice data are stored in the VPBM 934 and a masking scheme is implemented such that only voice data is extracted from the VPBM 934.

Accordingly, based on the foregoing, it appears that *Tsztoo* describes voice data and non-voice data are stored in the VPBM in such a way that the voice data is not contiguous. As described above, the non-voice data in the VPBM is used to program the CAM and, thus, this non-voice data is not analogous to symbol data. Accordingly, *Tsztoo* is not analogous to claim 1, which recites a buffer memory for storing the symbol data for the logical channel according to input sequences so that the symbol data between logical channels are stored in a continuous arrangement.

Further, the Applicant notes that the Examiner also relies upon a second, different embodiment to continue rejecting claim 1. In particular, the Examiner contends that the "voice data is stored within the VPBM (buffer memory according to different channels, and is advantageously packed into a common packet (continuous arrangement) [refer column 9 lines 65-68, column 10 lines 1-4." *See the Office Action at p. 10.* However this description of *Tsztoo* is related to the ***second embodiment***, and not the third embodiment as the Examiner alleges. The second embodiment, which is related to FIGS. 4-8 of *Tsztoo*, "does not include a dedicated address generator" such as the channel address generator 924 in the third embodiment. *See Tsztoo at 7:19-20.* Furthermore, the second embodiment describes how "a contiguous memory space can be divided into non-contiguous portions[.]" *See Tsztoo at 10:18-19.* Accordingly, the second embodiment of *Tsztoo* is not analogous to claim 1, which recites a buffer memory for storing the symbol data for the logical channel according to input sequences so that the symbol data between logical channels are stored in a continuous arrangement.

Further, none of the cited art cure at least the above-noted deficiencies of *Tsztoo*. Thus, for at least the foregoing reasons, claim 1 and all claims depending therefrom would not have been obvious from *Tsztoo* applied alone or in any reasonable combination with *Kuehnel* and/or *Witkowski*. Further, claim 6 and all claims depending therefrom are patentable over the cited references for at least substantially the same reasons discussed above in connection with claim 1.

IV. Conclusion

The Applicant submits that the above amendments and arguments are fully responsive to the Office Action dated December 24, 2008. Further, the Applicant submits that, for at least the foregoing reasons, all pending claims are in condition for allowance and notice to that effect is requested. Should the Examiner have any questions, the Examiner is encouraged to contact the undersigned at the telephone number indicated below.

Respectfully submitted,

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